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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,157	03/09/2006	Toshiaki Takenaka	2006-0223A	3496

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EXAMINER	
GOFF II, JOHN L	

ART UNIT	PAPER NUMBER
1791	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,157	TAKENAKA ET AL.	
	Examiner	Art Unit	
	John L. Goff	1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/24/09 has been entered.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-4 and 6-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

5. Claim 1 as amended requires "wherein the thermal expansion coefficient of the pair of lamination plates is different from a thermal expansion coefficient of the metal foil". It is

unclear where in applicant specification the metal foil is disclosed as having a different thermal expansion coefficient than the lamination plates.

Claim Rejections - 35 USC § 103

6. Claims 1, 3, 6-9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Specification pages 1-4, 8, and 9) in view of Pommer (U.S. Patent 6,560,844).

The admitted prior art discloses a conventional method of manufacturing a multi-layer circuit board comprising providing a structure including a core circuit board having a circuit pattern thereon and a prepreg sheet having a through-hole filled with conductive paste sandwiched between a pair of metal foils further sandwiched between a pair of lamination plates and applying heat and pressure to form a laminated structure (Figures 6A-6D and Page 3, line 6 to Page 4, line 8). The admitted prior art does not specifically teach the lamination plates are selected to have a thermal expansion coefficient (TCE) equivalent to a TCE of the core circuit board. It was known in the art that each layer of the laminated structure, e.g. a structure including circuit board and prepreg layers as depicted in Figure 1, should have the same or approximately the same TCE and that the plate on which the layers are laminated is selected to have a TCE the same or approximately the same as that of the layers as shown by Pommer to prevent distortion of the layers (Figures 1 and 3 and Column 2, lines 3-5 and 44-49). Pommer teaches the TCE of the layers and plate need only be approximately the same to the extent that any misalignment caused by any difference in TCE falls within acceptable bounds. It would have been obvious to one of ordinary skill in the art at the time the invention was made to

practice the method as taught by the admitted prior art wherein all of the layers of the structure and the lamination plates have the same or approximately the same TCE to prevent distortion of the layers as taught by Pommer.

Regarding the limitation of "wherein, a thermal expansion coefficient of the pair of lamination plates is equivalent to a thermal expansion coefficient of the core circuit board", applicants specification defines the term "equivalent" on page 13, lines 17-20 as "In the description that selecting a lamination plate with a thermal expansion coefficient equivalent to that of a core circuit board, the "equivalent" coefficient means that the thermal expansion coefficient of a lamination plate has a permissible range of ±20 % with respect to that of a core circuit board.". This is the interpretation given the claim wherein the pair of lamination plates and core circuit board as taught by the admitted prior art as modified by Pommer having a TCE the same or approximately the same is considered within the broad range of ±20 % to each other.

Regarding the limitation of "wherein the expansion coefficient of the pair of lamination plates is different from a thermal expansion coefficient of the metal foil", the term "different" is interpreted as not identical. The admitted prior art teaches the pair of lamination plates are usually formed of material having a TCE equivalent to that of the metal foil. As shown above equivalent does not require identical such that the admitted prior art teaches the TCE of the lamination plate has a permissible range of ±20 % with respect to that of the metal foil such that the limitation is met. Further, the TCE is only usually equivalent such that the limitation is met when the TCE of the lamination plate and metal foil are not equivalent. Finally, the pair of lamination plates and metal foil as taught by the admitted prior art as modified by Pommer have

a TCE approximately the same but different to the extent that any misalignment caused by any difference in TCE falls within acceptable bounds such that the limitation is met.

Regarding claims 3 and 6, the admitted prior art teaches the core circuit board has four or more layers. The admitted prior art teaches the core circuit board and the prepreg sheet are alternately laminated so as to have two or more layers.

Regarding claims 7 and 8, the admitted prior art further teaches a buffer material considered formed of a material capable of accommodating differences in TCE between the lamination plate and a carrying plate disposed outside the structure which structure is placed on a heat press plate considered the carrying plate such that heat and pressure goes through the buffer material and the carrying plate. It would have been obvious to one of ordinary skill in the art at the time the invention was made to practice the method as taught by the admitted prior art wherein all of the layers in the lamination have the same or approximately the same TCE to prevent distortion of the layers as taught by Pommer thereby including selecting a carrying plate whose TCE is the same or approximately the same as the lamination plate.

Regarding claim 9, the admitted prior art teaches the prepreg sheet contains a base and a resin layer impregnated with the base to form a resin layer on both surfaces of the base.

Regarding claims 11 and 12, the admitted prior art as modified by Pommer is considered to require measuring the TCE of all of the layers including the core circuit board otherwise selecting a lamination plate with the same or approximately the same TCE would not be possible.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 6-9, 11, and 12 above, and further in view of Ikeguchi et al. (JP 57011026 and see also the abstract).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 2 except for a specific teaching that the thickness of the resin layer formed on both sides of the base is at least 20 microns in total thickness. Ikeguchi disclose a prepreg excellent in workability comprising a base and a resin layer impregnated with the base to form a resin layer on both sides of the base having at least 20 microns in total thickness (See the abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the resin layers on both sides of the base as taught by the admitted prior art as modified by Pommer with a thickness at least 20 microns in total as shown by Ikeguchi to form a prepreg excellent in workability.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 6-9, 11, and 12 above, and further in view of Shirasawa et al. (U.S. Patent 4,614,559).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 4 except for a specific teaching that the core circuit board is not less than one time as thick as the prepreg sheet. Shirasawa directed to manufacturing a multi-layer circuit board comprising core circuit boards and prepreg sheets teach the layers are desirably as thin as possible to form a dimensionally stable board including specifically demonstrating the core circuit boards are not less than one time as thick as the prepreg sheets (Column 1, lines 33-35 and Tables 1 and 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

use as the core circuit board and prepreg sheet in the admitted prior art as modified by Pommer layers as thin as possible including wherein the core circuit board is not less than one time as thick as the prepreg sheet as shown by Shirasawa to form a multi-layer circuit board that is thin and dimensionally stable.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 6-9, 11, and 12 above, and further in view of Del (U.S. Patent 4,180,608).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 10 except for a specific teaching that the base is woven and the resin is B-staged. It is considered extremely well known in the art that a prepreg generally comprises a woven base and a B-staged resin as evidenced by Del (Column 4, lines 23-27). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the prepreg taught by the admitted prior art as modified by Pommer as was generally well known including a woven base and a B-staged resin as evidenced by Del only the expected results being achieved.

10. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 6-9, 11, and 12 above, and further in view of Levit (U.S. Patent Application Publication 2005/0230072).

The admitted prior art and Pommer as applied above teach all of the limitations in claims 11-14 except for a specific teaching that the TCE for each layer is measured by measuring the TCE at two positions or more in a range from room temperature to a heat pressing temperature by using a thermomechanical measurement apparatus and calculating an average value of the TCE from the two positions or more, it being noted Pommer is not limited to any particular

technique for measuring the TCE for each layer. Levit is exemplary of measuring the TCE of a layer for use in a circuit board wherein determining the TCE for the layer includes measuring the TCE at two positions or more in range from room temperature to a heat pressing temperature by using a thermomechanical measurement apparatus and calculating an average value of the TCE from the two positions or more (Paragraphs 0011, 0030, and 0038). It would have been obvious to one of ordinary skill in the art at the time the invention was made to measure the TCE for each layer of the structure taught by the admitted prior art as modified by Pommer to determine that each layer has an equivalent TCE as required by Pommer wherein a known suitable technique for determining the TCE was disclosed by Levit.

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art and Pommer as applied to claims 1, 3, 6-9, 11, and 12 above, and further in view of Hashimoto et al. (U.S. Patent 6,492,030).

The admitted prior art and Pommer as applied above teach all of the limitations in claim 15 except for a specific teaching that the thickness of the prepreg is 70 μm, it being noted neither the admitted prior art nor Pommer is limited to any particular thickness. It is considered conventional in the art that a prepreg such as that used in the admitted prior art as modified by Pommer has a thickness of 30 to 100 μm as shown by Hashimoto (Column 2, lines 31-33). Absent any unexpected results, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the thickness of the prepreg in the admitted prior art as modified by Pommer a conventional thickness such as 70 μm as shown by Hashimoto only the expected results being achieved.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art, Pommer, and Hashimoto as applied to claim 15 above, and further in view of Del.

The admitted prior art and Pommer as applied above teach all of the limitations in claim 15 except for a specific teaching that the thickness of the prepreg after pressing is 60 μm, it being noted neither the admitted prior art nor Pommer is limited to any particular thickness. It is known that a prepreg after pressing results in a reduced thickness as shown by Del (Column 7, lines 33-35). Absent any unexpected results, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use as the thickness of the prepreg in the admitted prior art as modified by Pommer any conventional thickness such as 70 to 60 μm as shown by Hashimoto wherein the thicknesses are chosen as a function of the thickness of the prepreg reducing during pressing as evidenced by Del.

Response to Arguments

13. Applicant's arguments with respect to claims 1-4 and 6-16 have been considered but are moot in view of the new ground(s) of rejection.

Applicants argue, "In other words, although Pommer teaches that each layer 30 and the alignment plate 10 have a similar thermal expansion coefficient, Pommer still fails to disclose or suggest specifically that the thermal expansion coefficient of the core circuit board is similar to that of the pair of lamination sheets, as recited in claim 1.". and "As a result, according to the position asserted in the Office Action Pommer teaches that the metal foil and the lamination sheets have the same thermal expansion coefficient, but fails to disclose or suggest that the

thermal expansion coefficient of the pair of lamination plates is different from a thermal expansion coefficient of the metal foil, as recited in claim 1.".

The admitted prior art discloses a conventional method of manufacturing a multi-layer circuit board including a core circuit board sandwiched between a pair of metal foils further sandwiched between a pair of lamination plates and applying heat and pressure to form a laminated structure. The admitted prior art does not specifically teach the lamination plates are selected to have a thermal expansion coefficient (TCE) equivalent to a TCE of the core circuit board. Pommer evidences it was known in the art that each layer of the laminated structure should have the same or approximately the same TCE and that the plate on which the layers are laminated is selected to have a TCE the same or approximately the same that of the layers to prevent distortion of the layers. Pommer teaches the TCE of the layers and plate need only be approximately the same to the extent that any misalignment caused by any difference in TCE falls within acceptable bounds.

Regarding the limitation of "wherein, a thermal expansion coefficient of the pair of lamination plates is equivalent to a thermal expansion coefficient of the core circuit board", applicants specification defines the term "equivalent" on page 13, lines 17-20 as "In the description that selecting a lamination plate with a thermal expansion coefficient equivalent to that of a core circuit board, the "equivalent" coefficient means that the thermal expansion coefficient of a lamination plate has a permissible range of ±20 % with respect to that of a core circuit board.". This is the interpretation given the claim wherein the pair of lamination plates and core circuit board as taught by the admitted prior art as modified by Pommer having a TCE the same or approximately the same is considered within the broad range of ±20 % to each other.

Regarding the limitation of "wherein the expansion coefficient of the pair of lamination plates is different from a thermal expansion coefficient of the metal foil", the term "different" is interpreted as not identical. The admitted prior art teaches the pair of lamination plates are usually formed of material having a TCE equivalent to that of the metal foil. As shown above equivalent does not require identical such that the admitted prior art teaches the TCE of the lamination plate has a permissible range of ±20 % with respect to that of the metal foil such that the limitation is met. Further, the TCE is only usually equivalent such that the limitation is met when the TCE of the lamination plate and metal foil are not equivalent. Finally, the pair of lamination plates and metal foil as taught by the admitted prior art as modified by Pommer have a TCE approximately the same but different to the extent that any misalignment caused by any difference in TCE falls within acceptable bounds such that the limitation is met.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John L. Goff** whose telephone number is **(571)272-1216**. The examiner can normally be reached on M-F (7:15 AM - 3:45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on (571) 272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John L. Goff/
Primary Examiner, Art Unit 1791